UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/423,415	11/05/1999	SEISUKE MORIOKA	27877.00066	6706

7590 03/14/2003

JOSEPH R KEATING,ESQ
KEATING & BENNETT,LLP
10400 EATON PLACE SUITE 312
FAIRFAX, VA 22030

EXAMINER
BLACKMAN, ANTHONY J

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 03/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/423,415	Applicant(s) MORIOKA, SEISUKE	
	Examiner ANTHONY J BLACKMAN	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-20 and 22-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20 and 22-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. Objection to the title is withdrawn because title more clearly describes the instant application.

Claim Objections

2. Claim objection to claim 23 is withdrawn because applicant corrected minor error.

Response to Arguments

3. Applicant's arguments with respect to claims 11-20 and 22-34 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this

application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 11-20 and 22-34 are rejected under 35 U.S.C. 102(anticipated) as being anticipated by VAN HOOK et al, US Patent No. 6353438.

6. Consider claim 14. VAN HOOK et al disclose an apparatus for image processing (figures 10a and 10b), comprising: a processor including a data decompression circuit (figure 9, elements 904, 903 and 902, - the need for a decompression circuit – column 6, lines 51-53, column 8, line 65 to column 9, line 15); a first storage device having texture data and electronically coupled to said processor (figure 9, elements 904-proessor and storage devices 903 or 901)); a texture buffer having decompressed texture data and electrically coupled to said processor (figure 9 , element 908 couples 904 and 901); wherein transmission of texture data between said texture buffer electrically coupled to said processor is faster than transmission of texture data between said storage device and said processor (figure 9, column 6, lines 40-53, column 8, line 54 to column 9, line 15 discloses that element 903 transmits data faster than element 901).

7. Consider claim 15. VAN HOOK et al disclose an apparatus for image processing (figures 10a and 10b), comprising: a processor including a data decompression circuit (figure 9, elements 904, 903 and 902, - the need for a decompression circuit – column 6, lines 51-53, column 8, line 65 to column 9, line 15); a first storage device having texture data and electronically coupled to said processor (figure 9, elements 904-proessor and storage devices 903 or 901)); a texture buffer having decompressed texture data and electrically coupled to said

processor (figure 9 , element 908 couples 904 and 901); a first data bus(figure 9, element 909) and a second data bus (figure 9, element 908), wherein said first data bus carries texture data between said texture buffer and said processor faster than said second data bus carries texture data from said storage device and said processor (column 7, lines 51-63, column 8, line 54 to column 9, line, 15, 35-39, and column 10, lines 8-24 disclose the slower transfer by element 901 and the faster transfer by element 903).

8. Consider claim 23. VAN HOOK et al disclose an image processing method (column 17, lines 45-54) comprising the steps of: providing compressed texture data in a storage device (figure 9, elements 903 and 902); reading said compressed texture data from said storage device (figure 9, elements 904 and 903, column 10, lines 8-34) and decompressing said compressed texture data in a texture buffer (figure 9, element 904, 908, 901); storing said decompressed texture data between said texture buffer and said processor faster than transferring data between said storage device and said processor (column 7, lines 51-63, column 8, line 54 to column 9, line, 15, 35-39, and column 10, lines 8-24 disclose the slower transfer by element 901 and the faster transfer by element 903).

9. Consider claim 11. VAN HOOK et al meet limitations for claim 14, in addition to the following limitation; further comprising a frame buffer, wherein said processor stores image data in said frame buffer (column 10, lines 14-24).

10. Consider claim 12. VAN HOOK et al meet limitations for claim 14, in addition to the following limitation; wherein said processor reads decompressed

texture data contained in said texture buffer (column 10, lines 8-16) and performs image processing of said decompressed texture data for conversion to image data (column 10, lines 16-34).

11. Consider claim 13. VAN HOOK et al meet limitations for claim 14, in addition to the following limitation; wherein said processor reads compressed texture data from said first storage device (column 10, lines 8-16), said data decompression circuit decompresses said read compressed texture data (figure 9, elements 904 and 901), and said processor stores said decompressed texture data in said texture buffer (column 10, lines 25-34).

12. Consider claim 16. VAN HOOK et al meet limitations for claim 13, in addition to the following limitation; wherein said processor includes a FIFO storage device which temporarily stores said read compressed texture data (column 6, lines 33-39).

13. Consider claim 17. VAN HOOK et al meet limitations for claim 16, in addition to the following limitation; wherein said data decompression circuit receives said compressed texture data from said FIFI storage device (column 6, lines 33-39).

14. Consider claim 18. VAN HOOK et al meet limitations for claim 13, in addition to the following limitation; wherein said processor includes a palette transformation circuit (figure 9, element 904) transformation circuit performing palette transformation of said decompressed texture data (column 10, lines 8-34).

15. Consider claim 19. VAN HOOK et al meet limitations for claim 13, in addition to the following limitation; wherein said processor includes a mip map generation circuit (column 4, lines 8-36), said mip map generation circuit generating a mip map of said decompressed texture data (column 4, lines 8-34).

16. Consider claim 20. VAN HOOK et al meet limitations for claim 14, in addition to the following limitation; wherein said texture data in said first storage device is compressed (figure 9, element 903 and 902).

17. Consider claim 22. VAN HOOK et al meet limitations for claim 23, in addition to the following limitation; further comprising the step of converting said decompressed texture data to image data, and storing said image data in a frame buffer (column 4, lines 14-24).

18. Consider claim 24. VAN HOOK et al meet limitations for claim 23, in addition to the following limitation; further comprising the step of performing palette conversion of said processor faster than said transferring data between said storage device and said processor (column 10, lines 24-34).

19. Consider claim 25. VAN HOOK et al meet limitations for claim 23, in addition to the following limitation; further comprising the step of generating a mip map of said compressed texture data prior to said step of storing said decompressed texture data (column 6, lines 33-39).

20. Consider claim 26. VAN HOOK et al meet limitations for claim 23, in addition to the following limitation; wherein said step of storing said decompressed data includes the step of updating said decompressed texture

data in said texture buffer with new decompressed texture data (column 2, lines 30-41, column 13, line 63 to column 14, line 28).

21. Consider claim 27. VAN HOOK et al meet limitations for claim 15, in addition to the following limitation; further comprising a frame buffer, wherein said processor stores image data in said frame buffer (column 10, lines 14-24).

22. Consider claim 28. VAN HOOK et al meet limitations for claim 15, in addition to the following limitation wherein said processor reads decompressed texture data contained in said buffer and performs image processing of said decompressed texture data for conversion to image data (column 10, lines 8-24).

23. Consider claim 29. VAN HOOK et al meet limitations for claim 15, in addition to the following limitation; wherein said processor reads compressed texture data from said first storage device (column 10, lines 8-16), said data decompression circuit decompresses said read compressed texture data (figure 9, elements 904 and 901), and said processor stores said decompressed texture data in said texture buffer (column 10, lines 25-34).

24. Consider claim 30. VAN HOOK et al meet limitations for claim 29 in addition to the following limitation; wherein said processor includes a FIFO storage device which temporarily stores said read compressed texture data (column 6, lines 33-39, further, it is inherent that the FIFO device will temporarily store data).

25. Consider claim 31. VAN HOOK et al meet limitations for claim 30, in addition to the following limitation; wherein said data decompression circuit

receives said read compressed texture data from said FIFO storage device (column 6, lines 12-53).

26. Consider claim 32. VAN HOOK et al meet limitations for claim 29, in addition to the following limitation; wherein said processor includes a palette transformation circuit (figure 9, element 904) transformation circuit performing palette transformation of said decompressed texture data (column 10, lines 8-34).

27. Consider claim 33. VAN HOOK et al meet limitations for claim 29, in addition to the following limitation; wherein said processor includes a mip map generation circuit (column 4, lines 8-36), said mip map generation circuit generating a mip map of said decompressed texture data (column 4, lines 8-34).

28. Consider claim 34. VAN HOOK et al meet limitations for claim 15, in addition to the following limitation; wherein said texture data in said first storage device is compressed (figure 9, element 903 and 902).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANTHONY J BLACKMAN whose telephone number is 703-305-0833. The examiner can normally be reached on FLEX SCHEDULE.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MATTHEW BELLA can be reached on 703-308-6829. The fax phone numbers for the organization where this application or proceeding

is assigned are 703-872-9314 for regular communications and 703-746-5731 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

ANTHONY J BLACKMAN
Examiner
Art Unit 2676

***

March 10, 2003

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600